DATUMTE.015A PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Taylor, et al.	Art Unit: 2186
App. No.	:	10/732,998	
Filed	:	December 11, 2003	
For	:	CACHE MEMORY ARCHITECTURE AND ASSOCIATED MICROPROCESSOR DESIGN	
Examiner	:	Hetul Patel	

AMENDMENT AND SUBSTANCE OF INTERVIEW

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed on December 14, 2005, please reconsider the above-referenced application in view of the following amendments and remarks.

AMENDMENTS TO THE SPECIFICATION

Please revise the specification as follows:

Paragraph beginning at page 4, line 5:

There are also definite physical barriers to desired cache implementations. The size of a cache memory built on a microprocessor chip is limited by the costs and yield loss resulting from larger die sizes. Off chip caches may more easily accommodate large cache sizes, but are limited by the restrictions on number of microprocessor chip pins that can be practically used to transfer addresses and data between the processor and the memory system. Further, a multiplicity of chips ~~may required~~ may be required to implement the off-chip cache resulting in increased system cost.

Paragraph beginning at page 5, line 25:

RAM manufacturers have also made efforts to reduce the costs of tag RAMs used for off-chip cache implementations. These efforts focus on aspects of the manufacturing of the cache data and cache tag RAM chips. For example, U.S. Patent No. 5,905,996, granted on May 18, 1999, discloses a cache design in which the tag memory is included within the same integrated circuit chip as the data memory. This approach allows the memory supplier to provide the tag and data functionality without the expense of manufacturing two separate parts. This allows the manufacturer to target the most cost effective array sizes in a given technology. This dual function chip is still somewhat specialized in that it includes the appropriate tag functionality as specified by the system requirements. As a result, these dual-function RAM devices are likely to be significantly more expensive ~~that~~ than general purpose RAMs traditionally used for cache data arrays.

Paragraph beginning at page 10, line 3:

In the illustrated embodiment of Figure 5, the comparator 40 generates a tag match signal 42 that is passed to the system controller **[[44]]** 35 to indicate whether the requested data resides in the level 2 cache 30. As is conventional, the system controller may abort the memory read operation if a tag match (cache hit) occurs. As described below, rather that relying on a microprocessor-generated tag match signal to make this determination, the system controller 35 may be designed to latch the cache tag as it is read from the cache memory bank 30, and perform its own comparison of the this cache tag to the main memory address.

AMENDMENTS TO THE DRAWINGS

Please replace the informal drawing sheets filed with the present application with the enclosed set of replacement drawings sheets.